REMARKS

Claims 1-4 and 6-21 were examined and rejected. Applicants amend claims 8 and 11 and cancel claims 14 and 23. Applicants submit that no new matter is added therein, as the amendments are supported by claim 14, Figures 2-4 and paragraphs 15-21 of the application as originally filed. Applicants respectfully request reconsideration of claims 1-4, 6-13, 15-16, 20-22 and 24-25 in view of the following remarks.

I. Claims Rejected Under 35 U.S.C. § 102

The Patent Office rejects claims 1-2 and 6-7 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,119,192 to Kao et al. (Kao). It is axiomatic that to be anticipated every limitation of the claim must be disclosed in a single reference.

Applicants respectfully disagree with the rejection above and submit that claim 1 is patentable over the cited references for at least the reason that the cited references do not disclose wherein the non-volatile memory has a maximum memory size less than a memory size sufficient to fill all the configuration registers, as required by claim 1. According to claim 1, for example, the maximum size of the memory is not large enough to store all of the address information and data corresponding to the address information for all of the configuration registers of the device. Hence, less than all of the plurality of configuration registers of the device can be loaded using the data in the memory.

Kao discloses an interface and memory for providing second initialization parameters from a supplemental parameter memory separate and distinct from the system BIOS memory (see column 2 lines 63-67). Specifically, Kao teaches that "any one or more of the initialization registers can be configured in any desired sequence," (see column 3 lines 13-15) and that the BIOS or supplemental initialization parameters can be used to configure the registers (see column 3 lines 17-20), including a method where a supplemental initialization procedure may be enabled to initialize the controller circuit, or otherwise, if such supplemental initialization procedure is not enabled, initialization of the controller circuit is accomplished using registers from a system BIOS during a normal system boot up routine (see column 3 lines 20-40). Hence, as the Patent Office notes in the final paragraph of page 3 of the current Office Action, the memory has a size equal to a memory size sufficient "to fill some or all of the configuration registers." Thus, since the memory has a size sufficient to fill all of the

configuration registers, it does not have a maximum memory size less than a memory size sufficient to fill all of the configuration registers, as required by claim 1.

Hence, Applicants respectfully request the Patent Office withdraw the rejection above.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious for at least the same reasons given above in support of their base claims.

II. Claims Rejected Under 35 U.S.C. § 103

The Patent Office rejects claims 3-4 under 35 U.S.C. § 103(a) as being unpatentable over Kao in view of U.S. Patent Application Serial No. 2004/0143715 to Bonaccio et al. (Bonaccio).

Claim 3 and 4 are submitted as not being anticipated or obvious for at least the same reasons given above in support of their base claims. Hence, Applicants respectfully request the Patent Office withdraw the rejection above for claims 3-4.

The Patent Office rejects claims 8-10 under 35 U.S.C. § 103(a) as being unpatentable over Kao in view of Bonaccio and U.S. Patent No. 6,480,946 to Tomashima et al. (Tomashima). To render a claim obvious, every limitation of that claim must be taught or suggested by at least one properly combined reference.

Applicants respectfully disagree with the rejection above and submit that claim 8 is patentable over the cited references for at least the reason that the cited references do not teach or suggest repeating the resetting and loading to repeat a multi-stage test data loading process with subsequent test information stored in the non-volatile memory during a memory design validation stage, as required by amended claim 8. As noted by the Patent Office in item 50 of page 15 of the current Office Action, neither cited reference Kao or Bonaccio teach this limitation of amended claim 8. Specifically, Kao teaches setting up and configuring a PCI/ISA interface using a conventional system BIOS/CPU initialization cycle (see column 2 lines 36-41). Similarly, Bonaccio teaches reconfiguring an integrated circuit by retrieving and loading register settings (see Abstract).

Similarly, Tomashima teaches reducing skew between read and write signals of a memory system including a plurality of discrete memory devices connected in parallel to a bus to transmit/receive signals to and from a commonly provided controller (see column 1 lines 7-15; column 6 lines 44-53). Also, Tomashima teaches a conventional memory controller performing this reduction by sending a command signal to Vernier circuit 300a during initialization of the memory devices (see column 6 lines 60-65; column 7 lines 30-33) during normal operational mode (see column 37 lines 33-39; column 8 lines 57-62; column 36 line 26 through column 37 line30; and column 38 lines 1-4).

Consequently, the Patent Office has not identified and Applicants are unable to find any teaching or suggestion in the references of repeating the resetting of a plurality of configuration registers and loading the registers according to information including address information and data corresponding to the address information during a memory design validation stage, as required by amended claim 8. As recited in amended claim 8, the terms "during a memory design validation stage" are only to exclude normal operational mode of a conventional system that does not repeat resetting and loading, to repeat a multi-stage test data loading process with subsequent test information stored in a nonvolatile memory during a memory design validation stage.

Hence, Applicants respectfully request the Patent Office withdraw the rejection above.

In addition to the reasons above, Applicants submit that the motivation for combining Tomashima with Bonaccio or Kao is improper. Specifically, Bonaccio and Kao teach programming configuration registers using configuration sets stored in BIOS. On the other hand Tomashima teaches adjusting reference voltage Vref of a Vernier circuit to reduce skew between read and write signals to and from discrete memory devices of a memory system (see Figures 43 and 46; and column 35 line 28 through column 37 line 55). Specifically, Vref is updated using tap circuit 300a which includes a shift register circuit 315, gates, latches and switches (see column 38) which may be initialized by a command applied from the memory controller (see column 37 lines 1-10). Thus, there is no motivation or suggestion in Tomashima for resetting configuration registers and loading configuration registers using information stored in a nonvolatile memory. Consequently, the motivation for such a combination can be

gleaned only from Applicants' specification. Hence, the combination is improper. Therefore, for at least this additional reason, Applicants respectfully request the Patent Office withdraw the rejection above.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious for at least the same reasons given above in support of their base claims.

The Patent Office rejects claims 11-13 and 16 under 35 U.S.C. § 103(a) as being unpatentable over Bonaccio in view of Kao.

Applicants respectfully disagree with the rejection above and submit that independent claim 11 is patentable over the cited references for at least the reason that the cited references do not teach or suggest loading at least two of the plurality of registers according to the test information during a memory design validation stage, wherein the test information includes a plurality of test address information and a plurality of test data corresponding to the plurality of test address information, each of the plurality of test address information identifying at least one of the plurality of registers to which a corresponding test data should be written; identifying a subset of the plurality of test data that corresponds to a subset of the plurality of registers having default data values equal to desired data for achieving the desired configuration prior to loading, as required by claim 11.

With respect to the "during a memory design validation stage" limitation of amended claim 11, an argument analogous to the one above with respect to claim 8 applies here as well. Hence, for at least the first reason that the cited references do not teach or suggest that limitation, Applicants respectfully request the Patent Office withdraw the rejection above.

Next, to address, the above noted "identifying a subset of the plurality of test data that corresponds to a subset of the plurality of registers having default data values equal to desired data for achieving the desired configuration prior to loading" limitations, the Patent Office relies upon paragraph 23 and Figure 1 of Bonaccio which shows a chip having a register memory that may be programmed, and describes configuration set 142 including one or more settings for any number of the registers. Moreover, Bonaccio teaches three scenarios for the configuration set: initialize all configuration sets; initialize or replace a single configuration set; or initialize selected

parts of a configuration set (see paragraph 29), such as to specify setting values which program specific characteristics (see paragraph 4) to be used during normal operations of the chip (see paragraph 5).

However, the Patent Office has not identified and Applicants are unable to find any teaching or suggesting in Bonaccio of loading registers according to the test data; and identifying a subset of test data that correspond to a subset of registers having default data values equal to desired data for achieving a desired configuration, as required by claim 11. According to amended claim 11, for instance, test data written over the default values in the registers during design is identified as corresponding to registers that reset to desired data. In other words, for example, the reset data written over was the better or desired data (e.g., see paragraph 33 of Applicants' specification). In some cases, the desired data is overwritten with inferior test data, and the resulting inferior configuration is detected, thus identifying the reset data value as the desired value (e.g., the actual design will not include overwriting the reset value with the inferior test value). Bonaccio does the opposite as the data loaded corresponds to the registers that do not include desired data, or correspond to registers that are initialized to a desired setting where the default value is the correct one. Instead, Bonaccio teaches selecting and using configuration sets of data to write over non-desired configuration data (e.g., from reset), but does not teach identifying test data corresponding to registers having default values equal to desired data for achieving a desired configuration, as required by claim 11.

Hence, Applicants respectfully request the Patent Office withdraw the rejection above.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious for at least the same reasons given above in support of their base claims.

The Patent Office rejects claims 20-22 under 35 U.S.C. § 103(a) as being unpatentable over Kao in view of Bonaccio and U.S. Patent No. 5,737,524 to Cohen et al. (Cohen).

Applicants respectfully disagree with the rejection above for at least the reason that the cited references do not teach or suggest wherein the non-volatile memory has a

maximum memory size less than a memory size sufficient to fill all the configuration registers, as required by independent claim 20.

An argument analogous to the one above with respect to claim 1 and Kao applies here as well.

Likewise, Bonaccio teaches initializing all configuration sets (see paragraph 29), but does not teach or suggest a maximum memory size as noted above for claim 20.

Also, Cohen teaches loading configuration registers with information which is stored in a non-volatile storage (see column 2 lines 59-64). However, the Patent Office has not identified and Applicants are unable to find any teaching or suggestion in Cohen of the above noted maximum memory size limitation of claim 20.

Thus, none of Kao, Bonaccio, Cohen or their combination teaches or suggests the above noted limitation of claim 20.

Hence, Applicants respectfully request the Patent Office withdraw the rejection above.

The Patent Office rejects claims 14 and 17-19 under 35 U.S.C. § 103(a) as being unpatentable over Kao and Bonaccio as applied to claim 11, and further in view of Tomashima.

Claim 14 has been canceled and its limitations included in claim 11. Also, claims 17-19 depend from claim 11, and hence are allowable for at least the reasons given above in support of their independent claim. Thus, Applicants respectfully request the Patent Office withdraw the rejection above.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious for at least the same reasons given in support of their base claims.

III. Claims 24-25

Applicants note that the Patent Office has not provided a specific rejection for claims 24 and 25.

CONCLUSION

In view of the foregoing, it is believed that all claims now are now in condition for allowance and such action is earnestly solicited at the earliest possible date. If there are any additional fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666.

Respectfully submitted,

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Dated: 10/18/06

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Suzanne Johnston — 10/18/06 Date